

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE	
In re application of: Bruce B. Doris et al.	Date: April 20, 2007
Serial Number: 10/604,190	Examiner: Tu Tu V. Ho
Filed: 06/30/2003	Group Art Unit: 2818 Confirmation No.: 1189
Title: HIGH PERFORMANCE CMOS DEVICE STRUCTURES AND METHOD OF MANUFACTURE	IBM Corporation D/18G, B/321, Zip 482 2070 Route 52 Hopewell Junction, NY 12533-6531

LETTER TO OFFICIAL DRAFTSPERSON

Commissioner of Patents and Trademarks
Alexandria, VA 22313

Dear Sir:

Responsive to the Examiner's comment #3, attached is a replacement Drawing sheet showing a corrected Figure 3(b).

Corrected Figure 3(b) clarifies width "transistor region R" described in paragraph 34 of the specification as filed.

Further, element 80 as shown in Figure 3(b) is a tensile barrier etch stop layer 80 described, e.g., in paragraph 33 of the specification as filed.

Respectfully submitted,
Bruce B. Doris et al.

By: _____

(Signature)
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20 Apr. 2007